What to consider when selecting the optimal test strategy

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Abstract
With today's test and inspection technologies more options are available. In the last couple of years Solder Paste Inspection (SPI), Automatic Optical Inspection (AOI), and Automatic X-ray inspection have become very significant complements to electrical test such as In-Circuit Test (ICT) and Functional Test (FT). With all of these valid options which is the optimal test strategy?

This paper will answer that question by addressing several issues for selecting the optimal inspection strategy, presenting data from many studies Agilent has performed in the quest to find the optimal test / inspection strategy. Some of the key conclusions from all the studies are that for process control one should test / inspect as early as possible. For defect containment, however, one should test / inspect as late as possible, since a significant number of defects are introduced very late in the manufacturing process. One additional parameter of selecting the optimal test strategy is board complexity. The paper will address all these issues, present data from the studies we have performed and include a short discussion on economic test models which are important to use when selecting the optimal test strategy.

Introduction
Today's test engineers have significantly more challenges than just a few years ago. The board complexity is increasing with more components, more joints, higher densities, new package technologies such as area array packages, and 0402 and 0201 chip components. The higher component and joint counts create more defect opportunities which lead to lower yields for a given defect level. At the same time, there are more test and inspection alternatives today with new technologies such as Solder Paste Inspection (SPI), Automatic X-ray Inspection (AXI), and Automatic Optical Inspection (AOI). These inspection technologies are well established and provide real choices today. Boundary-Scan test technology has also emerged as a popular electrical technique to complement In-Circuit Test (ICT) and Functional Test (FT). While these new tools offer more choices, they also pose a new dilemma. Which is the right test / inspection strategy? Which is the optimal combination of these tools?

This paper will focus on that question. Agilent Technologies has performed many studies trying to find out industry defect levels[1][2], we have done test effectiveness studies [3][4] with the purpose of finding out different test / inspection methods' effectiveness of finding different defects and we have done studies trying out different combination of test strategies to see how they complement each other [5][6]. Some results of these studies have confirmed what is already known in the industry. Some have shown new results not known in the industry, and some results have even been opposite common beliefs in the industry. The new findings and the surprising results have resulted in discussions and new insights. This paper will discuss the key findings in the studies we have done. It will also present the new insights and conclusions we have made. It will discuss different important areas when selecting the optimal test strategy and it will also discuss different economic models and how our new learnings can be incorporated into economic justifications.

Faults, defects, process indicators and potential defects
These terms are important when selecting test strategies and it is important to have a clear understanding of what they are. Therefore they will be defined and explained. Definitions will be in italic and underlined:

A Fault is a manifestation of a defect. An example is a digital device output pin that does not toggle correctly. For simplicity think about a two input OR-gate whose output is stuck high. This is a fault and is a manifestation of a defect. The causing defect can be any one of several: among others, a defective component, a wrong placed component, an open input pin, an open output pin. The fault class is a subset of the defect class. Electrical test such as In-Circuit (ICT), Boundary-Scan, and Functional Test (FT) are mainly detecting faults.

A defect is, at the end of the manufacturing process, an unacceptable deviation from a norm. The fault described above is also a defect, but there may be defects that are not showing up as faults. Examples

are insufficient solder, a misaligned component, a missing bypass capacitor and an open power pin. Inspection systems such as Automatic Optical Inspection (AOI), and Automatic X-ray Inspection (AXI) are detecting many of the defects and also some of the same faults as electrical test.

Defects, which also includes the faults, need to be corrected before the product is shipped.

A process indicator is, at the end of the manufacturing process, an acceptable deviation from a norm. Good examples are insufficient solder or misaligned components. The insufficient solder is not insufficient enough that it renders a repair action. However if many of these conditions exist, a process improvement action may be required.

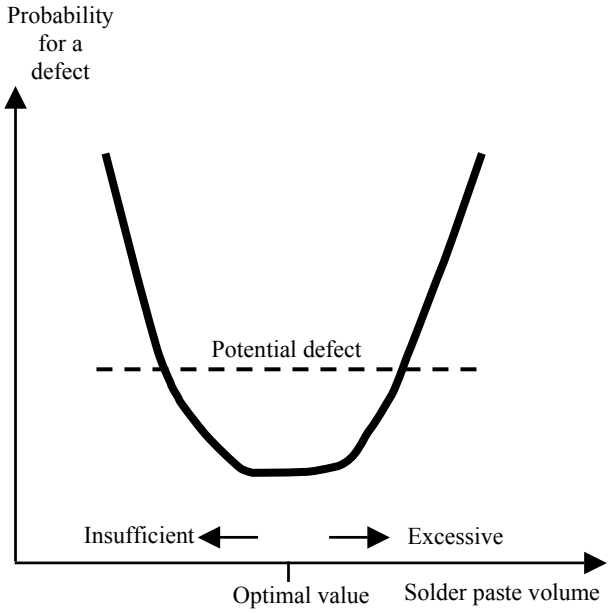

Figure 1. The concept of a potential defect, potential defects may or may not be defects at the end of the manufacturing process.

A potential defect is, in the manufacturing process, a deviation from a norm, that may or may not be a defect at the end of the manufacturing process. This is a new category and needs to be understood. An example is a pre-reflow misaligned chip component. This component may or may not self-align in the reflow oven. Another example is an insufficient paste volume that may not end up as a defective solder joint at the end of the manufacturing process [7]. Is it then important to keep track of these types of potential defects? The answer is yes and it is easiest explained by looking at figure 1. This example is also around solder paste volume. There is an optimal paste volume value that creates the fewest defects down the line. If the paste volume decreases, the probability for defects down the manufacturing line increases. Also as the paste volume increases from the optimal value, the probability for a defect down the line increases. For process control it is important to tune the process to the optimal value. However if only a few solder pads on a board have solder paste volume below a threshold it may not be optimal to clean the board and re-paste it. Remember that we are talking about potential defects.

Test and inspection engineers at the end of the line are mainly interested in finding the faults and defects. Process engineers that are responsible for improving the manufacturing process are mainly interested in potential defects, process indicators, and systematic defects.

Defect levels in the industry

There are frequent claims made in the industry that companies have defects at the rate of only 50 – 100 Parts Per Million (PPM) or Defects Per Million Opportunities (DPMO). Our studies suggest that these defect levels are probably obtained only on the board types with the lowest defect levels and probably only on a "good" day when everything is working to the advantage of that company. The average actual defect levels are typically significantly higher. A key point is that optimal test strategy is very different if the general defect levels are around 50 DPMO versus 500 DPMO. A very comprehensive study [1], with production data from about six months of production at fifteen different companies and over one billion solder joints in the study, indicated an average defect level of between 650 to 1,100 DPMO. These numbers are probably closer to the real defect numbers in the industry, especially on medium and high complexity boards that are manufactured in smaller batches. The European SMART PPM Monitoring Project also reports these higher defect levels. PPM levels for the month of December can be seen in figure 2 [8].

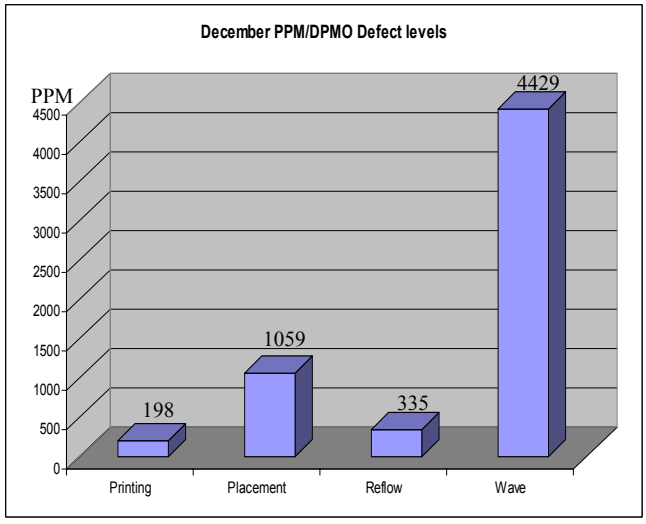

Figure 2. European SMART Group PPM Monitoring Project, December 2002 values.

Board types manufactured in higher volumes on the same SMT line for several days typically have lower defect levels, between 200 DPMO to 600 DPMO, because process adjustments can be made to achieve lower defect levels.

The DPMO levels in "the one billion solder joint study" are stated on a joint basis. One solder joint is one defect opportunity and there can be either zero or maximum one defect per solder joint.

In addition to understanding defect levels and the defect spectrum, it is also important to have knowledge of where in the manufacturing process that defects are introduced and can be detected. Much of this knowledge has been gained through Test Effectiveness studies, so this will be addressed in the next section.

Test Effectiveness studies

If defect levels are typically higher than commonly claimed, next we need to address the test effectiveness of major inspection and test technologies. This can be done with a Test Effectiveness study. The Test Effectiveness study is done on a smaller sample of boards, typically between 20 to 100 boards. The lower number is used if the study is done on a very complex board with many defect opportunities. The higher number of boards is used for medium complexity boards with fewer defect opportunities. For optimum results a total of 100 to 200 defects should be found. The same set of boards is tested / inspected by different methods, such as AOI and / or AXI, ICT, and sometimes Functional Test.

If we are doing a Test Effectiveness study of AOI, AXI, and ICT, the boards are first inspected by the AOI system. All calls that the AOI system makes are classified as either true defects or false calls. A log is kept of all defects classified as true defects, but they are not repaired at this time. In the test effectiveness studies, typically only one defect per component is counted, even if, for example, one QFP component has three open pins. After AOI the boards go to the AXI system and we repeat the process. All AXI calls, classified as true defects, are noted in the log. Again no repairs are done at this time. Typically many of the defects found by the AOI system are also found by the AXI system. There are usually a few defects detected by the AOI system that the AXI system did not detect; however there are typically many defects found by AXI that AOI did not detect.

After AXI the boards go to the ICT system and are tested again. Again at ICT we are trying to isolate the true defects from false calls. Since ICT is the last step in our example study, we can now start to do repairs. In a Test Effectiveness study we are only keeping track of defects (and faults), and not of process indicators and potential defects. It is also important to note that it is not the engineers from the ATE vendor (Automatic Test Equipment) who make the judgment on what is a defect and what is not. This is done by the CMs' and / or OEMs' engineers.

Let's assume that after this process we have found a total of 100 defects. Let's also assume the AOI system found 62 of those defects, the AXI system found 91 of the defects, and the ICT system 54. Then the AOI system's Test Effectiveness is 62% (62 out of a total of 100 known defects), the AXI Test Effectiveness is 91%, and the ICT 54%.

Generally a Test Effectiveness study takes 3 to 5 working days to perform, not including any program preparation that may be needed. It is very important to keep very good track of each defect, and it is better to limit the number of boards in the study than to compromise the integrity of the data. A Test Effectiveness study, executed correctly, is almost always a big eye opener and is strongly recommended to do every third or fourth year or when any new, significant changes in test strategy are considered.

Case Study 1

The effectiveness of each test / inspection system will vary from shop to shop and even from assembly type to assembly type. The data presented in this paper is being shared in an attempt to show the usefulness of a Test Effectiveness study and to share some insights on effectiveness and where defects are introduced in the manufacturing process.

This first data is a compilation of two Test Effectiveness studies. These two studies included AOI post-reflow, AXI, and ICT. In these two cases, no hand-load and solder wave process were included, therefore AOI, AXI, and ICT were all at the same manufacturing process. In these two studies there were a total of 80 boards inspected / tested and a total of 200 defects identified by the systems and confirmed by the CM. AOI was able to detect 127 out of the total of 200 defects, resulting in a test effectiveness of 64%. AXI was able to detect 163 defects, resulting in a test effectiveness of 82%. ICT found 116 of all defects, resulting in a test effectiveness of 58%.

Case Study 2

This study was performed to compare AOI to AXI and also to gain some insights on where the optimal placement of these inspection systems would be, depending on where defects were introduced. It should be noted that this study is focused on detecting defects. The study is not trying to gain insights into how test and inspection can be used to

improve the process. The current test strategy includes ICT. The AOI, AXI, and ICT were performed after the following process steps (see table 1).

Process step	AOI	AXI	ICT
Post pick-and-place, Pre-reflow	X		
Post-reflow, Pre-wave	X	X	
Post-wave		X	X

Table 1

The first data is presented in Figure 3, a Venn diagram showing the defect coverage for each tester. The AOI circle represents all defects found by the AOI at both inspection points. Likewise the AXI circle includes any defect found at either AXI step.

We can see that in the current test strategy, ICT is only catching 22% of all defects. Adding AOI to this test process will increase the test effectiveness to 46%. Or adding AXI to ICT will increase the test effectiveness to 95%.

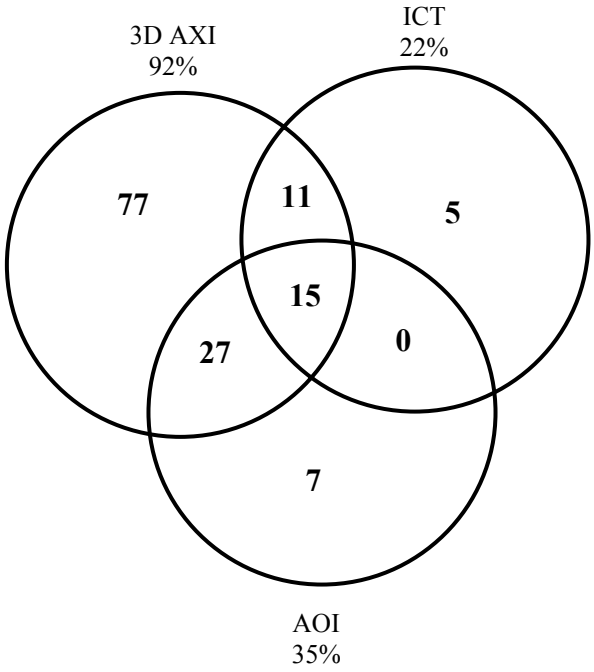

Figure 3. Defects found by AOI, AXI, and ICT.

Next we look more closely at the AOI and AXI results at each process step. AOI pre-reflow was detecting 4 defects and AOI post-reflow was detecting 48 defects. From this we can see that AOI post-reflow was more effective than AOI pre-reflow to detect final defects. It should be noted that pre-reflow AOI detected many potential defects and process indicators, for instance misaligned components, that were corrected at the reflow process. The AOI pre-reflow could have contributed significantly at process improvements and adjustments of the placement machines.

AXI was done both pre-wave and post-wave. Pre-wave detected 72 defects and post-wave AXI detected 125 defects. Here we saw that AXI is more effective post-wave than pre-wave, because the wave (or selective wave) process is introducing a significant number of defects, in this case around 40% of all defects. That should also be taken into consideration when the test effectiveness of the AOI is judged. 40% of the defects were introduced after the AOI inspection.

We have seen very similar results, namely that the wave process introduces significant numbers of defects, from the special test effectiveness studies we have done when analyzing a test strategy of maximum 3D x-ray with a limited or reduced ICT test [6]. In one of these studies, defects introduced at the hand-load and selective wave-process accounted for over 55% of final defects. In the other studies, we did not specifically keep track of this number but on average around 50% of all defects appear to be introduced at the wave process.

These case studies illustrate that a significant number of defects are detectable only after reflow and also that the wave or selective wave introduces almost half of all defects. It highlights the importance of good defect containment as late as possible in the manufacturing line.

The studies we have performed have mainly been focused on defect containment. We have only counted defects that were still defects at the end of the manufacturing line. However we have also noticed a significant number of process indicators and potential defects in these studies.

Where in the manufacturing process are defects introduced?

As discussed in the previous section, the reflow oven can be seen as a defect transformation box. Many defects go into the reflow oven and many defects come out of the reflow oven, but they may not always be the same ones. Examples of defects that change are: misaligned parts that self-align, insufficient solder that can make acceptable joints, parts that fall off, apparently good parts that do not solder, solder bridges that open up, and open areas that get bridged. At the same time some defects are the same both before and after the reflow oven. Examples are: missing parts that are still missing, parts with no solder paste that will not solder and will be open, gross misalignments that will still be misaligned, reversed parts that will still be backwards, and some misaligned that are still misaligned. So for defect containment it is best to place the inspection system after the reflow oven. For optimal process control and for detecting placement defects of expensive

components the optimal inspection system position is pre-reflow.

We also saw in the previous section that a wave or selective wave process contributes around 50% of all defects. For this reason it is best to place the inspection system after the wave process for maximum defect containment.

Field failures and warranty costs

It is obvious that the selected test / inspection strategy will have an impact on the number of defects found by the end customer and also on warranty costs. An analysis of different test strategies impact on warranty defects for real production has been presented in other papers [5]. In short, selecting the right test strategy could decrease the number of warranty defects by almost an order of magnitude.

Complexity

Another factor that impacts the test strategy selection is the board complexity. However the term "high complexity board" is very subjective. One company may be producing boards with over 30,000 solder joints and several thousand components on double-sided boards, while another company produces a single-sided board with fewer than 1,000 solder joints and under a hundred components. Both these companies may claim that these boards were "high complexity boards." It is obvious that the complexity of these two boards is very different. To provide a way to talk about board complexity in a more objective way, a Complexity Index was introduced in 1999 [5]. The original Complexity Index was calculated using number of components, number of joints, number of board sides, and low volume – high volume production batches. The objectives for the Complexity Index were to be very easy to calculate and to give a good indication of the complexity of the board. One key enhancement request has been that some form of component density or joint density should be included in the Index. Therefore a new, updated Complexity Index is suggested as:

$$Ci = ((\#C + \#J)/100) * S * M * D$$

Ci = Complexity Index
#C = Number of components
#J = Number of joints
S = Board sides (1 for double sided, and ½ for single sided)
M = Mix (1 for high mix, and ½ for low mix)
D = Density ((joints / square inch)/100) or
(joints / square cm / 15.5)

If the resulting Complexity Index is below 50 it is considered a low complexity board. If it is between 50 and less than 125 it is a medium complexity board, and if it is above or equal to 125 it is a high complexity board [9].

There are other factors that contribute to the complexity of a board, but, these key considerations keep the Complexity Index simple enough for everybody to find the numbers necessary for the calculation and then obtain the right "ball park" indication of the board's complexity. A final caveat: this index refers to complexity from a manufacturing point of view, not from a testing point of view. In manufacturing, the higher the complexity, the more difficult it is to achieve high yields without any test and inspection. Board complexity is an important parameter when selecting test strategy.

The following example, of a low complexity board and a high complexity board, illustrates significant differences in expected yield and need for different test strategies. Table 2 describes the key characteristics of each board.

	Low complexity	High complexity
Joints	1,000	20,000
Components	100	3,000
Sides	Double	Double
Mix/Volume	High mix	High mix
Density	80 j/inch2	80 j/inch2
Complexity Index	8.8	184
DPMO = 200	Yield = 80%	Yield = 1%
DPMO = 500	Yield = 58%	Yield = 0%
DPMO = 200	0.22 def./b.	4.6 def./b.
DPMO = 500	0.55 def./b.	11.5 def./b.

Table 2

The low complexity board has 100 components, 1000 joints, and has therefore 1,100 defect opportunities. The high complexity board has 3,000 components, 20,000 joints and has therefore 23,000 defect opportunities. If we assume that both board types are double sided, have a low volume / high mix characteristic and a joint density of 80 joints / square inch, then the complexity index for first board is 8.8 and 184 for the second board.

If we first assume a defect level of 500 DPMO then the yield of the low complexity board will be around 58% and the yield of the high complexity board will be around 0%. These yield calculations are using the formula:

Yield = (1- (DPMO/1,000,000))^Defect opportunities

The yield calculation estimates the raw yield out of the SMT manufacturing line without any test and inspection. The low complexity board will have an average of 0.55 defects per board and the high complexity board will have an average of 11.5 defects per board. From these numbers it is obvious that the high complexity board needs and can afford a more elaborate test / inspection strategy.

This example can also be used to illustrate the value of process control. Let us assume that we use process control and DFM (Design For Manufacturability) to lower the average defect levels from 500 DPMO to 200 DPMO. The impact of this process improvement can also be seen in table 2. The yield increase for the low complexity board is from 58% to 80%. The yield increase on the high complexity board is only 1%, but more importantly the average number of defects per board goes from 11.5 to 4.6. In both cases significant improvements can be achieved if test and inspection are also used for process improvements.

General test strategy recommendations

From the data presented in this paper we can come to some general conclusions.

If the main objective is to improve the process and have shorter process feedback, the focus of the test strategy should be early in the manufacturing process. However if the main objective is to improve defect containment, the focus of test strategy should be at the end of the PCBA (Printed Circuit Board Assembly) manufacturing process. These strategies are not mutually exclusive and efforts should be made in both areas. The process engineers are typically involved in improving the process and should be focused on process indicators and potential defects. Their objective should be to lower the overall defect levels at the end of the process. However, even if the process engineers are doing an outstanding job, there will always be some random defects and test / inspection engineers should be concerned with how to put strategies in place to find those defects. The objective should be for all manufacturing defects to be found prior to functional and system test, in order to have the highest yield possible into functional test. Finding manufacturing defects is more expensive, and functional test is typically not very effective at finding such defects, increasing the probability that those defects will escape to the end customer and cause increases in warranty costs.

The second general recommendation is that board complexity should have a big impact on the test strategy selection. The recommendation is that the higher the complexity, the more elaborate test strategy is needed. For very low complexity boards manufactured in low to medium volumes, a test strategy of only functional test may be the optimal test strategy. On the other extreme, for a very high complexity board with more than 30,000 solder joints, a test strategy of AOI, AXI, and ICT before functional test may be the most cost effective strategy. In this case all three test / inspection methods may be implemented at the end of the manufacturing line for defect containment. In addition inspection may be implemented for process control.

Economic Test Strategy Models

For a more sophisticated selection of the optimal test strategy, an economic model should be used. Many companies have this type of a model. These type of models are typically done in a spreadsheet program such as Microsoft Excel or Lotus 1-2-3.

The model allows inputs for yields or DPMO values out of the manufacturing process, board volumes, board cost etc. These models most often compare two test strategies against each other. The two different test strategies can be described, by entering values for test effectiveness, test cost, diagnosis and repair costs, programming cost, and fixture costs, etc. The models then calculate the total cost of the different strategies. It is often easy to change some of the input values and immediately see the impact. A good example of this type of tool is one that was developed by the NEMI Test Strategy Project and is also presented in this year's APEX conference. This model can be obtained free of charge from NEMI [10]. For this type of model to be accurate, accurate input data is a requirement. However it can be a valuable tool even if not 100% accurate data is available. If that is the case, the recommendation is, to use the best estimated input values possible. A sensitivity analysis should then be run to identify the most important input value(s). For the most sensitive information extra efforts should be made to find the most accurate values for these parameters. If after doing this sensitivity analysis and double checking the most sensitive numbers, one test strategy shows significantly more economic advantages, then the correct solution has been identified. However if there are only marginal differences between the two test strategies, a definite answer can not be found with that type of model. It should be understood that this type of model will only produce "ball-park" values, mainly because of the difficulties in providing accurate input values to the model.

Improvements to the general economic model

The concept of the general economic model was developed more than ten years ago and it should be clear that it is doing a good job of calculating economic impact, especially if different test / inspection strategies after the last major step in the

manufacturing process are evaluated. However recently Solder Paste Inspection systems (SPI) that keep up with the manufacturing line are available. Also AOI systems are available both pre-reflow and post-reflow. In the different studies we have performed we have also seen that defects are introduced during different manufacturing steps. Also we have seen that potential defects pre-reflow can change during reflow so they are no longer defects after the reflow oven. We are also aware that different types of test / inspection systems have different capabilities to detect different types of defects. For example we know that ICT is very good at detecting solder shorts, but not so good at detecting insufficient solder defects. Inspection systems are good at finding structural defects but not capable of finding components with electrical defects. From the above discussion we can see that the following improvements to the general economic model would be beneficial. First the concept that defects are introduced and changed during the manufacturing process should be supported. Second, it should be possible to describe where in the manufacturing process a test / inspection step is placed. Third, more than a general defect level and coverage number should be supported. For example it should be possible to describe different defect types such as opens, shorts, insufficient solder joints, missing components, electrical defective components etc., their individual defect levels and where in the manufacturing process those defects are introduced. In addition the different test / inspection systems' defect coverage for the different defect types should be considered. So for example we know that a missing component defect can only be detected after the placement operation, and Solder Paste Inspection (SPI) will not be able to detect that defect. In a similar fashion, inspection systems placed pre-wave will not be able to detect defects that are introduced in the wave process. The impact of different defects on the end customer should also be considered. For example an electrically defective component will have a higher probability of being detected by the end customer, than an insufficient solder joint. So the new improved tool should be able, for each different defect type, to calculate defect coverage and escape rates. For this improved tool to do correct calculations it is essential that correct data be available to plug into the model. As with any of this type of tool "garbage-in data" will result in "garbage-out results". This improved model requires more resolution of data than the general economic model. Because of this there is definitely a place for both models. If less data is available the general economic model will do a good job of calculating economic impact of different test strategies. However if data with more resolution is available, then the new improved economic model will do a better job of demonstrating impact of different test strategy selections.

Summary and conclusions

To select the optimal test strategy it is important:

- to understand the difference of faults, defects, process indicators, and potential defects.

- to have accurate data on defect levels and defect spectrum. Defect levels are typically higher than normally acknowledged in the industry.

- to have accurate data on test effectiveness of different test / inspection solutions. It is recommended that each test engineering department conduct a test effectiveness study at least every three or four years.

- to have knowledge where in the manufacturing process different defects are introduced and where they can be detected.

- if possible, to gather data from field returns and estimate different test strategies' impact on warranty costs.

- to include the board's complexity in the test strategy selection process.

- to have a holistic view of the test strategy, both from a process improvement point of view, as well as a defect containment point of view. It is also important that both of these major strategies be present.

- for process control with short feedback loops, the test / inspection system should be placed early in the manufacturing process.

- for optimal defect containment, the test / inspection system should be placed after the whole PCBA has been manufactured.

- for optimal test strategy selection an economic model should be used, either of the general type or the improved type described in the paper.

- continuous improvement in data gathering for optimal test strategy selection should be strived for and also continuous improvement in economic models used.

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